DDR4 SDRAM-SODIMM

4GB based on 4Gbit (512Mx8) component

Revision 1.0 (SEPT., 2014)
-Initial Release

Products and specifications discussed herein are subject to change without notice
© 2006 Super Talent Technology, Corporation.

1. Features

- Power Supply: VDD=1.2V (1.14V to 1.26V)
- VDDQ = 1.2V (1.14V to 1.26V)
- VPP - 2.5V (2.375V to 2.75V)
- VDDSPD=2.25V to 2.75V
- Functionality and operations comply with the DDR4 SDRAM datasheet
- 16 internal banks
- Bank Grouping is applied, and CAS to CAS latency (tCCD_L, tCCD_S) for the banks in the same or different bank group accesses are available
- Data transfer rates: PC4-2133, PC4-1866, PC4-1600
- Bi-Directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL8 or BC4(Burst Chop)
- On-Die Termination (ODT)
- Temperature sensor with integrated SPD
- This product is in compliance with the RoHS directive.
- Per DRAM Addressability is supported
- Internal Vref DQ level generation is available
- Write CRC is supported at all speed grades
- DBI (Data Bus Inversion) is supported(x8)
- CA parity (Command/Address Parity) mode is supported

2. Ordering Information

Part Number	Density	Organization	Component Composition	# of Rank	Description
F21SA4GS	4GB	512Mx64	512Mx8 x 8pcs	1	PC4-17000

Note: Last character of the Part Number (x) represents DRAM vendor
S=Samsung; M=Micron; H=Hynix

3. Key Timing Parameters

	DDR4-2133	Unit
CL-tRCD-tRP	15-15-15	tCK
CAS Latency	14.06	tCK
tCK(min)	0.93	ns
tRCD(min)	14.06	ns
tRP(min)	14.06	ns
tRAS(min)	33	ns
tRC(min)	47.06	ns

4. Address Configuration

Organization	Row Address	Column Address	Bank Address	Bank Group Address	Auto Pre-Charge
512Mx8(4Gb) base	A0-A14	A0-A9	BA0-BA1	BG0-BG1	A10/AP

Products and specifications discussed herein are subject to change without notice
© 2006 Super Talent Technology, Corporation.

5. DIMM Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR4 modules. Pins listed below may not be all supported on this module. Please see Pin Assignments for information specific to this module.

Pin Name	Description	Pin Name	Description
A0-A17[1]	Register address input	SCL	I^2C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I^2C serial data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0-SA2	I^2C slave address select for SPD/TS and register
RAS_n[2]	Register row address strobe input	PAR	Register parity input
CAS_n[3]	Register column address strobe input	VDD	SDRAM core power
WE_n[4]	Register write enable input		
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	12V	Optional power supply on socket but not used on RDIMM
CKE0, CEK1	Register clock enable lines input	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	Register on-die termination control lines input	VSS	Power supply return (ground)
ACT_n	Register input for activate input	VDDSPD	Serial SPD/TS positive power supply
DQ0-DQ63	DIMM memory data bus	ALERT_n	Register ALERT_n output
CB0-CB7	DIMM ECC check bits	VPP	SDRAM Supply
TDQS9_t-TDQS17_t TDQS_c-TDQS17_c	Dummy loads for mixed populations of x4 based and x8		
DQS0_t-DQS17_t	Data Buffer data strobes (positive line of differential pair)	RESET_n	Set Register and SDRAMs to a Known State
DBI0_n-DBI8_n	Data Bus Inversion	EVENT_n	SPD signals a thermal event has occurred
CK0_t, CK1_t	Register clock input (positive line of differential pair)	VTT	SDRAM I/O termination supply
CK0_c, CK1_c	Register clock input (negative line of differential pair)	RFU	Reserved for future use

1. Addrewss A17 is only valid for 16Gbx4 based SDRAMs.
2. RAS_n is a multiplexed function with A16
3. CAS_n is a multiplexed function with A15
4. WE_n is a multiplexed function with A14

6. Input/Output Functional Descriptions

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained highthroughout read and write accesses. Input buffers, excluding CK, CK_c, ODT, and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID: Chip ID is only used for 3DS for 2, 4, 8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code.

Products and specifications discussed herein are subject to change without notice
© 2006 Super Talent Technology, Corporation.

Symbol	Type	Function
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t,NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_c, DQSU_t, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multifunction. For example, for activation with ACT_n Low, those are Addressing like A16, A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table.
DM_n/DBI_n/ TDQS_t, (DMU_n/DBIU_n), (DML_n/DBIL_n)	Input / Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8.
BG0 - BG1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. x4/8 have BG0 and BG1 but x16 has only BG0.
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provided the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Auto-precharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Auto-precharge; LOW: no Auto-precharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}.

Products and specifications discussed herein are subject to change without notice
© 2006 Super Talent Technology, Corporation.

Symbol	Type	Function
DQ	Input/ Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t, and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11, 12, 10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW.
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. IF there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until ongoing DRAM internal recovery transaction to complete.
TEN	Input	Connectivity Test Mode Enable: Required on x16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable boundary scan operation along with other pins. It is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
NC		No Connect: No internal electrical connection is present.
V_{DDQ}	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.2 V +/- 0.06 V
V_{SS}	Supply	Ground
V_{PP}	Supply	DRAM Activation Power Supply: 2.5V (2.375V min , 2.75 max)
V_{REFCA}	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

Note: Input only pins (BG0-BG-1, BA0-BA1, A0-A17, ACT_n, RAS_n,/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.

Products and specifications discussed herein are subject to change without notice
© 2006 Super Talent Technology, Corporation.

7. Pin Assignments

260-Pin DDR4 SODIMM Front								260-Pin DDR4 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	67	DQ29	133	A1	199	DM5_n/ DBI5_n	2	V_{SS}	68	V_{SS}	134	EVENT_n, NF	200	DQS5_t
3	DQ5	69	V_{SS}	135	V_{DD}	201	V_{SS}	4	DQ4	70	DQ24	136	V_{DD}	202	V_{SS}
5	V_{SS}	71	DQ25	137	CK0_t	203	DQ46	6	V_{SS}	72	V_{SS}	138	CK1_t/NF	204	DQ47
7	DQ1	73	V_{SS}	139	CK0_c	205	V_{SS}	8	DQ0	74	DQS3_c	140	CK1_c/NF	206	V_{SS}
9	V_{SS}	75	DM3_n/ DBI3_n	141	V_{DD}	207	DQ42	10	V_{SS}	76	DQS3_t	142	V_{DD}	208	DQ43
11	DQS0_c	77	V_{SS}	143	PARITY	209	V_{SS}	12	DM0_n/ DBI0_n	78	V_{SS}	144	A0	210	V_{SS}
13	DQS0_t	79	DQ30	145	BA1	211	DQ52	14	V_{SS}	80	DQ31	146	A10/AP	212	DQ53
15	V_{SS}	81	V_{SS}	147	V_{DD}	213	V_{SS}	16	DQ6	82	V_{SS}	148	V_{DD}	214	V_{SS}
17	DQ7	83	DQ26	149	CS0_n	215	DQ49	18	V_{SS}	84	DQ27	150	BA0	216	DQ48
19	V_{SS}	85	V_{SS}	151	WE_n/ A14	217	V_{SS}	20	DQ2	86	V_{SS}	152	RAS_n/ A16	218	V_{SS}
21	DQ3	87	CB5/NC	153	V_{DD}	219	DQS6_c	22	V_{SS}	88	CB4/NC	154	V_{DD}	220	DM6_n/ DBI6_n
23	V_{SS}	89	V_{SS}	155	ODT0	221	DQS6_t	24	DQ12	90	V_{SS}	156	CAS_n/ A15	222	V_{SS}
25	DQ13	91	CB1/NC	157	CS1_n	223	V_{SS}	26	V_{SS}	92	CB0/NC	158	A13	224	DQ54
27	V_{SS}	93	V_{SS}	159	V_{DD}	225	DQ55	28	DQ8	94	V_{SS}	160	V_{DD}	226	V_{SS}
29	DQ9	95	DQS8_c	161	ODT1	227	V_{SS}	30	V_{SS}	96	DM8_n/ DBI_n/NC	162	C0/ CS2_n/NC	228	DQ50
31	V_{SS}	97	DQS8_t	163	V_{DD}	229	DQ51	32	DQS1_c	98	V_{SS}	164	V_{REFCA}	230	V_{SS}
33	DM1_n/ DBI_n	99	V_{SS}	165	C1, CS3_n, NC	231	V_{SS}	34	DQS1_t	100	CB6/NC	166	SA2	232	DQ60
35	V_{SS}	101	CB2/NC	167	V_{SS}	233	DQ61	36	V_{SS}	102	V_{SS}	168	V_{SS}	234	V_{SS}
37	DQ15	103	V_{SS}	169	DQ37	235	V_{SS}	38	DQ14	104	CB7/NC	170	DQ36	236	DQ57
39	V_{SS}	105	CB3/NC	171	V_{SS}	237	DQ56	40	V_{SS}	106	V_{SS}	172	V_{SS}	238	V_{SS}
41	DQ10	107	V_{SS}	173	DQ33	239	V_{SS}	42	DQ11	108	RESET_n	174	DQ32	240	DQS7_c
43	V_{SS}	109	CKE0	175	V_{SS}	241	DM7_n/ DBI7_n	44	V_{SS}	110	CKE1	176	V_{SS}	242	DQS7_t
45	DQ21	111	V_{DD}	177	DQS4_c	243	V_{SS}	46	DQ20	112	V_{DD}	178	DM4_n/ DBI4_n	244	V_{SS}
47	V_{SS}	113	BG1	179	DQS4_t	245	DQ62	48	V_{SS}	114	ACT_n	180	V_{SS}	246	DQ63
49	DQ17	115	BG0	181	V_{SS}	247	V_{SS}	50	DQ16	116	ALERT_n	182	DQ39	248	V_{SS}
51	V_{SS}	117	V_{DD}	183	DQ38	249	DQ58	52	V_{SS}	118	V_{DD}	184	V_{SS}	250	DQ59
53	DQS2_c	119	A12	185	V_{SS}	251	V_{SS}	54	DM2_n/ DBI2_n	120	A11	186	DQ35	252	V_{SS}
55	DQS2_t	121	A9	187	DQ34	253	SCL	56	V_{SS}	122	A7	188	V_{SS}	254	SDA
57	V_{SS}	123	V_{DD}	189	V_{SS}	255	V_{DDSPD}	58	DQ22	124	V_{DD}	190	DQ45	256	SA0
59	DQ23	125	A8	191	DQ44	257	V_{PP}	60	V_{SS}	126	A5	192	V_{SS}	258	V_{TT}
61	V_{SS}	127	A6	193	V_{SS}	259	V_{PP}	62	DQ18	128	A4	194	DQ41	260	SA1
63	DQ19	129	V_{DD}	195	DQ40	–	–	64	V_{SS}	130	V_{DD}	196	V_{SS}	–	–
65	V_{SS}	131	A3	197	V_{SS}	–	–	66	DQ28	132	A2	198	DQS5_c	–	–

Products and specifications discussed herein are subject to change without notice
© 2006 Super Talent Technology, Corporation.

8. Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.3 ~ 1.5	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

Note:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ. When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times

9. DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	NOTE
T_{OPER}	Normal Operating Temperature Range	0 to 85	°C	1,2
	Extended Temperature Range	85 to 95	°C	1,3

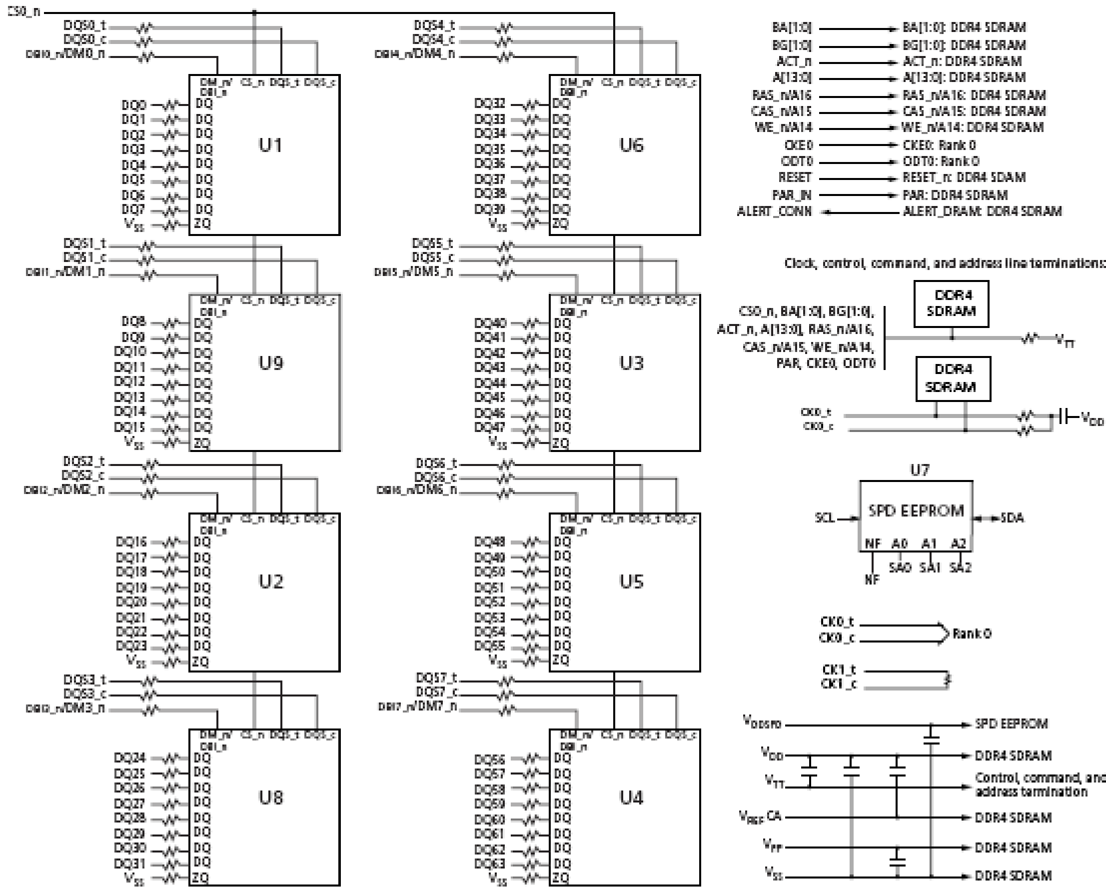
Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For mea- surement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. Dur- ing operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
    a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
    b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). DDR4 SDRAMs support Auto Self-Refresh and in Extended Temperature Range and please refer to component datasheet and/or the DIMM SPD for tREFI requirements in the Extended Temperature Range

© 2006 Super Talent Technology, Corporation.

SUPER ★ TALENT™
THE BEST MEMORY

10. Functional Block Diagram: 4GB; 512x64 Module (1R x8)



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

Products and specifications discussed herein are subject to change without notice
© 2006 Super Talent Technology, Corporation.

11. AC&DC Operating Conditions

Recommended operating conditions (Voltage referred to Vss=0V, TA=0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	1.14	1.2	1.26	V
V_{DDQ}	Supply Voltage for Output	1.14	1.2	1.26	V
V_{PP}		2.375	2.5	2.75	V

12. Input/Output Capacitance

Symbol	Parameter	DDR4-2133		DDR4-2400		Unit	NOTE
		min	max	min	max		
C_{IO}	Input/output capacitance	0.7	1.4	0.7	1.3	p	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	p	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c	-	0.05	-	0.05	p	1,2,3,5
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	p	1,3
C_{DCK}	Input capacitance delta CK_t and CK_c	-	0.05	-	0.05	p	1,3,4
C_{I}	Input capacitance(CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	p	1,3,6
C_{DI_CTRL}	Input capacitance delta(All CTRL pins only)	-0.1	0.1	-0.1	0.1	p	1,3,7,8
$C_{DI_ADD_CMD}$	Input capacitance delta(All ADD/CMD pins only)	-0.1	0.1	-0.1	0.1	p	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	p	1,3
C_{ZQ}	Input/output capacitance of ZQ	0.5	2.3	0.5	2.3	p	1,3,12
CTEN	Input capacitance of TEN	0.2	2.3	0.2	2.3	p	1,3,13

Note:

1. This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure TBD.
2. DQ, DM_n, DQS_T, DQS_c, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value CK_T-CK_C
5. Absolute value of CIO(DQS_T)-CIO(DQS_c)
6. CI applies to ODT, CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
7. CDI CTRL applies to ODT, CS_n and CKE
8. CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_T)+CI(CLK_C))
9. CDI_ADD_ CMD applies to, A0-A17, BA0-BA1, BG0-BG1,RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.
10. CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_T)+CI(CLK_C))
11. CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_T)+CIO(DQS_c))
12. Maximum external load capacitance on ZQ pin: tbd pF.
13. TEN pin may be DRAM internally pulled low through a weak pull-down resistor to VSS. In this case CTEN might not be valid and system shall verify TEN signal with Vendor specific information.

Products and specifications discussed herein are subject to change without notice
© 2006 Super Talent Technology, Corporation.

13.AC Timing Parameters & Specifications

(AC operating conditions unless otherwise noted)

Speed		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	8	-	8	-	ns	22
Average Clock Period	tCK(avg)	1.071	<1.25	0.938	<1.071	0.833	<0.938	ns	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_ to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)min + tJIT(per)min_ to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)min + tJIT(per)min _to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-54	54	-47	47	-42	42	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-27	27	-23	23	-21	21	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-43	43	-38	38	-33	33	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_tota l	107		94		83		ps	25
Cycle to Cycle Period Jitter determin-istic	tJIT(cc)_dj	54		47		42		ps	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	86		75		67		ps	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR(2per)	-79	79	-69	69	-61	61	ps	
Cumulative error across 3 cycles	tERR(3per)	-94	94	-82	82	-73	73	ps	
Cumulative error across 4 cycles	tERR(4per)	-104	104	-91	91	-81	81	ps	
Cumulative error across 5 cycles	tERR(5per)	-112	112	-98	98	-87	87	ps	
Cumulative error across 6 cycles	tERR(6per)	-119	119	-104	104	-92	92	ps	
Cumulative error across 7 cycles	tERR(7per)	-124	124	-109	109	-97	97	ps	
Cumulative error across 8 cycles	tERR(8per)	-129	129	-113	113	-101	101	ps	
Cumulative error across 9 cycles	tERR(9per)	-134	134	-117	117	-104	104	ps	
Cumulative error across 10 cycles	tERR(10per)	-137	137	-120	120	-107	107	ps	
Cumulative error across 11 cycles	tERR(11per)	-141	141	-123	123	-110	110	ps	
Cumulative error across 12 cycles	tERR(12per)	-144	144	-126	126	-112	112	ps	
Cumulative error across 13 cycles	tERR(13per)	-147	147	-129	129	-114	114	ps	
Cumulative error across 14 cycles	tERR(14per)	-150	150	-131	131	-116	116	ps	
Cumulative error across 15 cycles	tERR(15per)	-152	152	-133	133	-118	118	ps	
Cumulative error across 16 cycles	tERR(16per)	-155	155	-135	135	-120	120	ps	
Cumulative error across 17 cycles	tERR(17per)	-157	157	-137	137	-122	122	ps	
Cumulative error across 18 cycles	tERR(18per)	-159	159	-139	139	-124	124	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)						ps	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	100	-	80	-	62	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	200	-	180	-	162	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	125	-	105	-	87	-	ps	

Products and specifications discussed herein are subject to change without notice
© 2006 Super Talent Technology, Corporation.

Speed		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address Timing									
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	200	-	180	-	162	-	ps	
Control and Address Input pulse width for each input	tIPW	525	-	460	-	410	-	ps	
CAS_n to CAS_n command delay for same bank group	tCCD_L	5	-	6	-	6	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	Max(4nCK,3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	Max(4nCK,3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	Max(28nCK,30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,23ns)	-	Max(20nCK,21ns)	-	Max(20nCK,21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,17ns)	-	Max(16nCK,15ns)	-	Max(16nCK,13ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max (2nCK,2.5ns)	-		1,2,e,34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		1,34
Internal READ Command to PRE-CHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max (4nCK,7.5ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRCDM	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns	-	tWR+max (5nCK,3.75n s)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+ma x (5nCK,3.75ns)	-	tWTR_S+ma x (5nCK,3.75ns)	-	tWTR_S+m ax (5nCK,3.75n s)	-	ns	2, 29, 34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+m ax (5nCK,3.75n s)	-	ns	3,30, 34
DLL locking time	tDLLK	597	-	768	-	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-		
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	-	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))						nCK	
CS_n to Command Address Latency									
CS_n to Command Address Latency	tCAL	4						-	4

Products and specifications discussed herein are subject to change without notice
© 2006 Super Talent Technology, Corporation.

Speed		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
DRAM Data Timing									
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	TBD	-	TBD	-	TBD	tCK(avg) /2	13,18
DQS_t,DQS_c to DQ Skew determin- istic, per group, per access	tDQSQ	-	TBD	-	TBD	-	TBD	tCK(avg) /2	14,16,1 8
DQ output hold time from DQS_t,DQS_c	tQH	TBD	-	TBD	-	TBD	-	tCK(avg) /2	13,17,1 8
DQ output hold time deterministic from DQS_t, DQS_c	tQH	TBD	-	TBD	-	TBD	-	UI	14,16.1 8
DQS_t,DQS_c to DQ Skew total, per group, per access; DBI enabled	tDQSQ	-	TBD	-	TBD	-	TBD	UI	13,19
DQ output hold time total from DQS_t, DQS_c; DBI enabled	tQH	TBD	-	TBD	-	TBD	-	UI	13,19
DQ to DQ offset , per group, per ac- cess referenced to DQS_t, DQS_c	tDQSQ	TBD	TBD	TBD	TBD	TBD	TBD	UI	15,16
Data Strobe Timing									
DQS_t, DQS_c differential READ Pre- amble (2 clock preamble)	tRPRE	0.9	TBD	0.9	TBD	0.9	TBD	tCK	
DQS_t, DQS_c differential READ Postamble	tRPST	TBD	TBD	TBD	TBD	TBD	TBD	tCK	
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	tCK	21
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	tCK	20
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK	
DQS_t, DQS_c differential WRITE Postamble	tWPST	TBD	TBD	TBD	TBD	TBD	TBD	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-390	195	-360	180	-300	150	ps	
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	195	-	180	-	150	ps	
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	tCK	
MPSM Timing									
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCP- DED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCP- DED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)		tCKSRX(min)		tCK- SRX(min)	-		
Exit MPSM to commands not requir- ing a locked DLL	tXMP	TBD		TBD		TBD	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)		tXMP(min) + tXS- DLL(min)	-		
CS setup time to CKE	tMPX_S	TBD	-	TBD	-	TBD	-		
CS hold time to CKE	tMPX_H	TBD	-	TBD	-	TBD	-		

Products and specifications discussed herein are subject to change without notice
© 2006 Super Talent Technology, Corporation.

Speed		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Calibration Timing									
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing									
Exit Reset from CKE HIGH to a valid	tXPR	max (5nCK,tRFC(	-	max (5nCK,tRFC(min)+	-	max (5nCK,tRFC	-		
Exit Self Refresh to commands not re- quiring a locked DLL	tXS	tRFC(min)+1 0ns	-	tRFC(min)+1 0ns	-	tRFC(min)+ 10ns	-		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT (min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min) +10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min) +10ns	-		
Exit Self Refresh to commands requir- ing a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-		
Minimum CKE low width for Self re- fresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	tCKE(min)+1 nCK	-	tCKE(min)+ 1nCK	-		
Minimum CKE low width for Self re- fresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max (5nCK,10ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PA R	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10 ns)	-	max(5nCK,10 ns)	-	max (5nCK,10ns)	-		
Power Down Timing									
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-		
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-		31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR /tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+ 1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4D EN	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR /tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4 DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+ 1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	2	-	2	-	nCK	7

Products and specifications discussed herein are subject to change without notice
© 2006 Super Talent Technology, Corporation.

Speed		DDR4-1866		DDR4-2133		DDR4-2400		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
PDA Timing									
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)		max(16nCK,10ns)		max(16nCK, 10ns)			
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD			
ODT Timing									
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing									
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write level- ing mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/ DQS_n	tWLS	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t,	tWLH	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE							ns	
CA Parity Timing									
Commands not guaranteed to be exe- cuted during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	56	112	64	128	72	144	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	50	-	57	-	64	nCK	
Parity Latency	PL	4		4		5		nCK	
CRC Error Reporting									
CRC error to ALERT_n latency	tCRC_ALER T	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	nCK	
tREFI									
tRFC1 (min)	2Gb	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	ns	34
	16Gb	TBD	-	TBD	-	TBD	-	ns	34

Products and specifications discussed herein are subject to change without notice
© 2006 Super Talent Technology, Corporation.

Note:

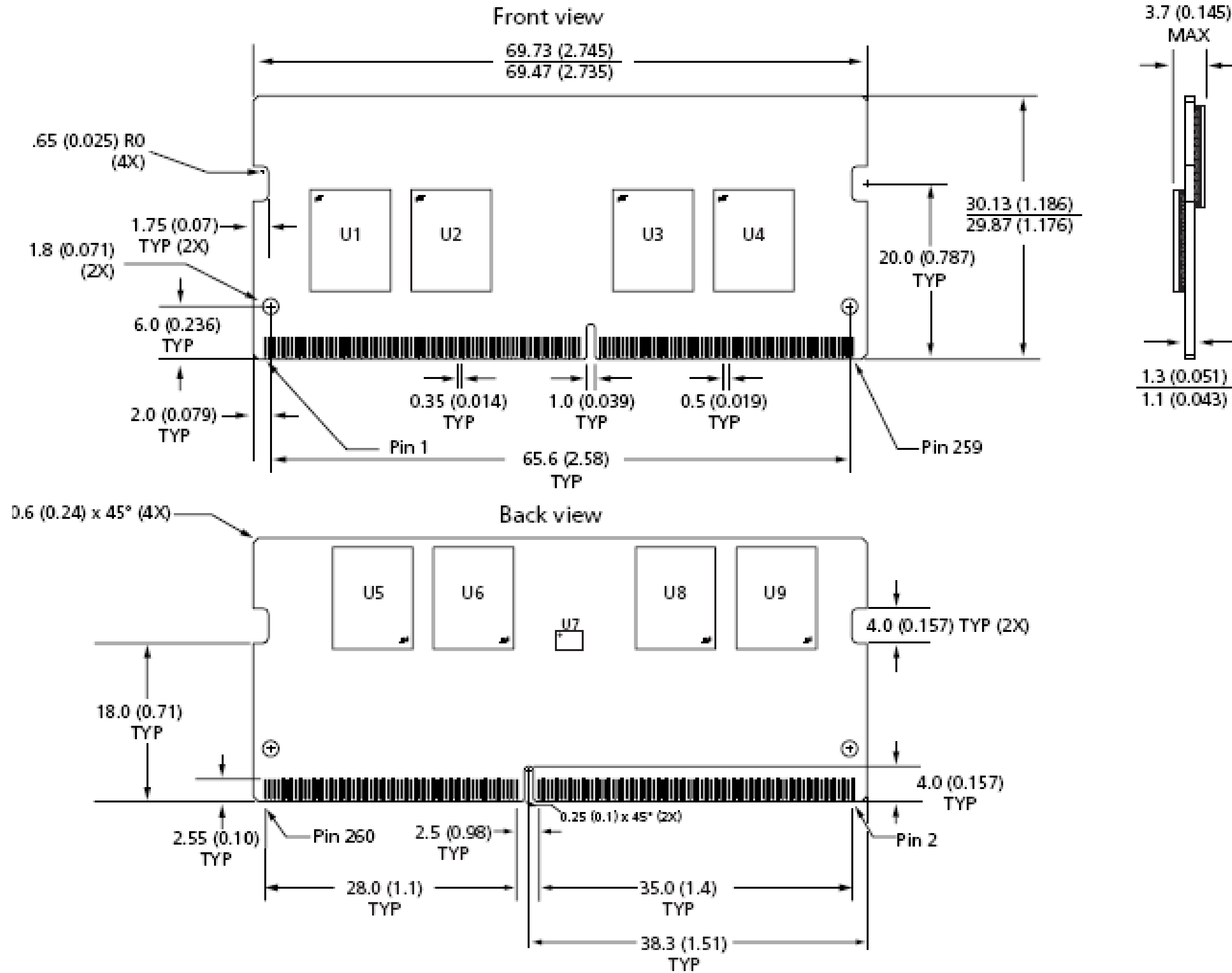
1. Start of internal write transaction is defined as follows :
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down
   IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables shown in section 10.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=tCK(avg).min/2

Products and specifications discussed herein are subject to change without notice
© 2006 Super Talent Technology, Corporation.

SUPER ★ TALENT
THE BEST MEMORY

14. Physical Dimensions: 512Mx64 Single Rank x8 (512Mx8 base)

Unit: Millimeters



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

* **NOTE** : Tolerances on all dimensions ±0.15 unless otherwise specified.

© 2006 Super Talent Technology, Corporation.